An Improved Analytical AC Large-Signal Model for the GaAs MESFET

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Abstract — Currently, the analysis of nonlinear microwave networks is a topic of much research effort and has produced many efficient and useful algorithms. To apply these algorithms, it is necessary to use an efficient model for each nonlinear device used. The modeling of MESFET's has been dealt with quite extensively in recent years, including a continuous effort by the author. In a recent publication, an efficient analytical model was presented. In the present paper, an improved model is described. The new model is basically the same as the previous one, except that a better expression is used for the conduction current calculation. The accuracy and applicability of the model are demonstrated by a set of simulation results and by comparison to measurement.

I. INTRODUCTION

IN RECENT YEARS the analysis of microwave nonlinear networks has been of great interest, and much research effort has been devoted to it, resulting in efficient analysis methods. Some commercial computer programs are already available, and more are expected in the near future. References [1]–[7] are examples of some of the recent publications on this topic.

Obviously, the GaAs MESFET is a useful microwave device, so it is important to have an efficient and accurate model for it. The author has developed in the past a field-theory-based model [8], [9], which relates the device physics and geometry to its electrical performance. Recently, a fully analytical approximation of the above model has been developed and published [10]. The above analytical model has been used extensively for simulation of amplifiers, mixers, frequency multipliers, etc., using the harmonic balance technique. As a result, some improvements to the above model are presented here. The improved model allows better correlation between simulated and measured performance. In Section II the improved model is presented and an accuracy evaluation involving the comparison of simulated and measured performance is described in Section III.

II. THE IMPROVED ANALYTICAL MODEL

A. General

The MESFET large-signal model is presented in Fig. 1. This figure is the same as in [10], and the description of the various elements of the network is given there, as well as in
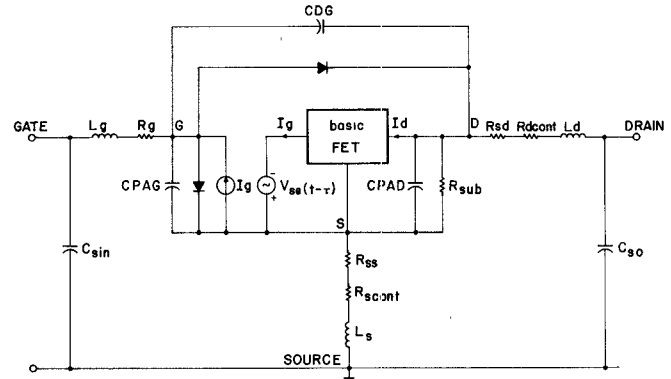
Fig. 1. Complete MESFET network.

[8] and [9] with a modification by Green [11]. The box labeled "basic FET" in Fig. 1 represents the active nonlinear portion of the device. This portion is the main part of the device and the most difficult to simulate accurately. The passive parasitic components can be either calculated from the device geometry by existing field-theory-based models or measured in a procedure described by Curtice [12]. The nonlinear portion, however, is best characterized by mathematical expressions:

$$I_g(t) = \text{GVSG}\frac{dV_{SG}(t - \tau)}{dt} + \text{GVDS}\frac{dV_{DS}(t)}{dt} \qquad (1)$$

$$I_D(t) = I_{con} + \text{DVSG}\frac{dV_{SG}(t - \tau)}{dt} + \text{DVDS}\frac{dV_{DS}(t)}{dt} \qquad (2)$$

where I_{con} is the drain–source conduction current. The other four parameters are capacitive coefficients representing the displacement current. The five variables are functions of the internal port voltages: $V_{SG}(t - \tau)$, $V_{DS}(t)$. This representation ((1) and (2)) is maintained over the entire dynamic range, including forward and avalanche conduction. This does not introduce an error, since the "basic FET" is practically shorted by the diodes when conduction occurs. Analytical expressions for the above five functions are presented in [10] in full detail in a form suitable for direct implementation by the reader. In this paper we present improved expressions for I_{con}, which better simulate this parameter. The four capacitive coefficients have not been changed, and they can be calculated by the expressions in [10].

B. The New Expressions for I_{con}

The improved expression for I_{con} is

$$I_{con} = I_S(1 + mV_{DS})\tanh(V_{DS}/V_S) \qquad (1)$$

where I_S, m, and V_S are functions of V_{SG}.

The physical meaning and expressions for the above functions are outlined below. I_S is the saturation current (same as I_{sat} in [10]). In the "old" model I_{sat} is calculated by expressions (5) in [10]. A better approximation has been derived as follows:

$$I_S = \begin{cases} I_{ON}, & V_{SG} < -V_F \\ A_1 V_{SG}^3 + A_2 V_{SG}^2 - g_{m0} V_{SG} + I_{DSS}, & -V_F \leqslant V_{SG} < 0 \\ A_3 V_{SG}^2 - g_{m0} V_{SG} + I_{DSS}, & 0 \leqslant V_{SG} < V_{gdsm} \\ A_4 V_{SG}^3 + A_5 V_{SG}^2 + A_6 V_{SG} + A_7, & V_{gdsm} < V_{SG} < V_{cut} \\ 0, & V_{cut} \leqslant V_{SG} \end{cases} \qquad (2)$$

where

$$A_1 = \frac{2(I_{ON} - I_{DSS})}{V_F^3} - \frac{g_{m0}}{V_F^2}$$

$$A_2 = \frac{3(I_{ON} - I_{DSS})}{V_F^2} - \frac{2g_{m0}}{V_F} \qquad (3)$$

$$A_3 = \frac{I_{DSm} - I_{DSS} + g_{m0}V_{gdsm}}{V_{gdsm}^2} \qquad (4)$$

$$A_4 = \frac{1}{(V_{cut} - V_{gdsm})^2}\left[\frac{2I_{DSm}}{V_{cut} - V_{gdsm}} + g_{m0} - 2\frac{I_{DSS} - I_{DSm}}{V_{gdsm}}\right] \qquad (5)$$

$$A_5 = \frac{I_{DSm} - A_4\left(V_{gdsm}^3 + 2V_{cut}^3 - 3V_{cut}^2 V_{gdsm}\right)}{(V_{cut} - V_{gdsm})^2} \qquad (6)$$

$$A_6 = -3A_4 V_{cut}^2 - 2A_5 V_{cut} \qquad (7)$$

$$A_7 = -A_4 V_{cut}^3 - A_5 V_{cut}^2 - A_6 V_{cut}. \qquad (8)$$

The meanings of the physical parameters are given in [10] (with the exception of I_{DSm}). I_{DSm} is the value of I_S for $V_{SG} = V_{gdsm}$. V_{gdsm} is the value of V_{SG} at which the drain conductance, g_d, is maximum. [Explanation: g_d approaches zero as V_{SG} approaches both $(-V_F)$ (open channel) and $V_{SG} = V_{cut}$ (cutoff), so there has to be a maximum for g_d at some value, V_{gdsm}, such that $-V_F < V_{gdsm} < V_{cut}$.] Expression (2) is a better approximation for I_S and includes five regions, rather than the four regions in the "old" model.

The physical meanings of m and V_S are determined by calculating the drain conductance by differentiating (1):

$$g_d = \frac{\partial I_{con}}{\partial V_{DS}} = G_{d_0}(1 + mV_{DS})\left[1 - \tanh^2\left(\frac{V_{DS}}{V_S}\right)\right]$$

$$+ G_{d_\infty}\tanh\left(\frac{V_{DS}}{V_S}\right) \qquad (9)$$

where

$$G_{d_0} = I_S/V_S \qquad (10)$$

$$G_{d_\infty} = mI_S. \qquad (11)$$

From (9) it is obvious that G_{d_0} is the value of g_d for $V_{DS} = 0$, namely, the initial slope of the $I-V$ curve. G_{d_0} is a function of V_{SG}. The suggested approximation for G_{d_0} is

$$G_{d_0} = G_{d_{00}}\left[1 - \sqrt{\frac{V_{SG} + \phi}{V_{cut} + \phi}}\right]\Big/\left[1 - \sqrt{\frac{\phi}{V_{cut} + \phi}}\right] \qquad (12)$$

where ϕ is the built-in potential of the gate junction ($\simeq 0.8$ V). G_{d_0} is proportional to the free channel height. $G_{d_{00}}$ is the value of G_{d_0} for $V_{SG} = 0$. V_S is calculated from (10) once G_{d_0} and I_S are known.

From (9) it is obvious that G_{d_∞} is the value of g_d for $V_{DS} \to \infty$. G_{d_∞} is a function of V_{SG}. The suggested approximation for G_{d_∞} is a polynomial expression identical to that of g_{ds} in [10, eq. (7)]. Once G_{d_∞} and I_S are known, m is calculated from (11).

C. Diode Characterization

The gate–source and gate–drain junctions are simulated in Fig. 1 by the pair of diodes. In the large–signal simulations the diodes are characterized by the following equation:

$$I_{diode} = I^*\left(e^{\beta V_{diode}} - 1 - e^{-\beta(V_{diode} + V_B)}\right) \qquad (13)$$

$$\beta = \frac{q}{kT} = 40 \qquad \text{(at room temperature)} \qquad (14)$$

where V_B is the avalanche breakdown voltage. I^* is generally not known; however, due to the exponential dependence on V_{diode} its exact value is not very important, and may be taken in the range of several nA. Equation (13) is basically the standard diode equation with the addition of a term representing the avalanche breakdown. The effect of "gradual avalanche" as described for example by Curtice [12] is not currently included in the diode model.

III. SIMULATION RESULTS

The accuracy and usefulness of the improved model are demonstrated in this section by presenting calculated versus measured data. The types of data presented are dc $I-V$ curves, small-signal scattering parameters, and large-signal simulation results.

The device chosen is the HMF1200 by HARRIS. This is a 0.5 W power device useful up to 16 GHz. It has 0.5 μm gate length, and is used for medium power applications. For this particular device, the electrical parameters used to characterize it by the improved analytical model are presented in Table I. The meaning of each of these parameters is explained in [10] with the necessary changes presented in Section II, above.

The dc I–V curves of the device are presented in Fig. 2 (calculated—solid line; measured—dashed line). The measured $I-V$ curves of a power MESFET always include a region of negative slope. This slope does not represent

TABLE I

MESFET HMF1200 DEVICE PARAMETERS TABLE

1	FORWARD CONDUCTION VOLTAGE (VF)	:	.50	VOLT
2	CUTOFF VOLTAGE (VCUT)	:	3.50	VOLT
3	VSG FOR MAX GDS (VGDSM)	:	2.00	VOLT
4	BUILT-IN POTENTIAL (PHI)	:	.80	VOLT
5	DEVICE MAX CURRENT (CURON)	:	430.00	MA
6	DEVICE CURRENT FOR VSG=0 (CURDSS)	:	340.00	MA
7	DEVICE CURRENT FOR VSG=VGDSM(CURDSM)	:	70.00	MA
8	GM FOR VSG=0	:	160.00	MMHO
9	GD VALUE FOR VSG=VDS=0 (GD00)	:	370.00	MMHO
10	GD VALUE FOR VSG=VGDSM (GDSM)	:	8.00	MMHO
11	GVSG VALUE FOR VSG=0 (CO)	:	1.793	PF
12	GVDS VALUE FOR VDS=VSG=0 (CMO)	:	0.4051	PF
13	(-DVSG) VALUE FOR LARGE VDS (CMAX)	:	0.0089	PF
14	DVDS VALUE FOR LARGE VDS (CH)	:	0.1372	PF
15	DVDS VALUE FOR VDS=0 (CL)	:	0.0443	PF
16	GVDS VALUE FOR LARGE VDS (CK)	:	0.0014	PF

MESFET HMF1200 PACKAGE/CIRCUIT PARAMETERS:

1	SOURCE INDUCTANCE (SIND)	:	2.27E-02	NANOHENRIES
2	GATE INDUCTANCE (GIND)	:	8.62E-02	NANOHENRIES
3	DRAIN INDUCTANCE (DIND)	:	2.14E-01	NONOHENRIES
4	PARASITIC INPUT CAPACITANCE (SCAPIN)	:	1.17E-03	PICOFARADS
5	PARASITIC OUTPUT CAPACITANCE (SCAPO)	:	3.17E-03	PICOFARADS
6	GATE PAD CAPACITANCE (CPADG)	:	2.58E-01	PICOFARADS
7	DRAIN PAD CAPACITANCE (CPADD)	:	2.78E-01	PICOFARADS
8	DRAIN TO GATE PAD CAPACITANCE (CAPDG)	:	1.08E-01	PICOFARADS
9	GATE METALLIZATION RESISTANCE (RG)	:	0.068	OHMS
10	SUBSTRATE LEAKAGE RESISTANCE (RSUBST)	:	1.00E+20	OHMS
11	SOURCE METALLIZATION RESISTANCE (RSCONT):		0.000	OHMS
12	DRAIN METALLIZATION RESITANCE (RDCONT)	:	0.000	OHMS
13	SOURCE BULK RESISTANCE (RSS)	:	0.589	OHMS
14	DRAIN BULK RESISTANCE (RSD)	:	0.881	OHMS
15	CHANNEL TIME DELAY (TAU)	:	4.150	PS

Fig. 3. S_{11} and S_{22} for HMF1200.

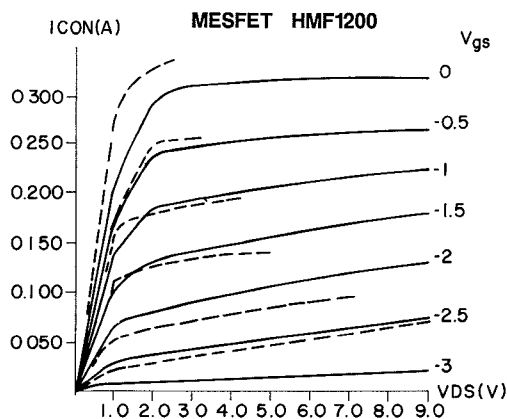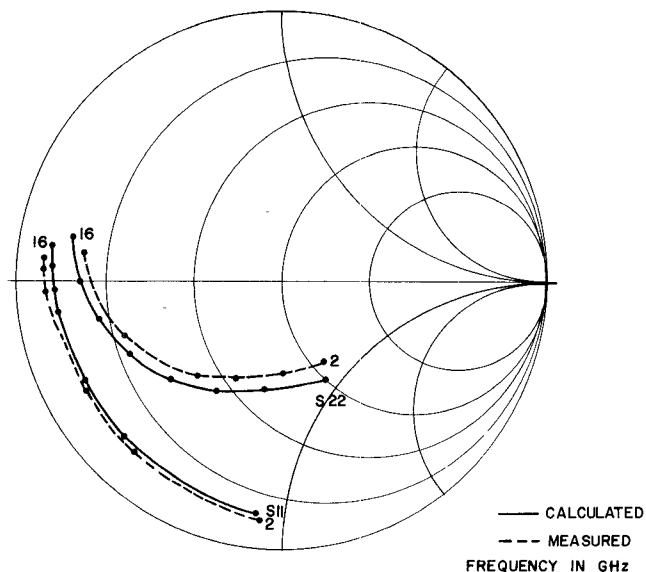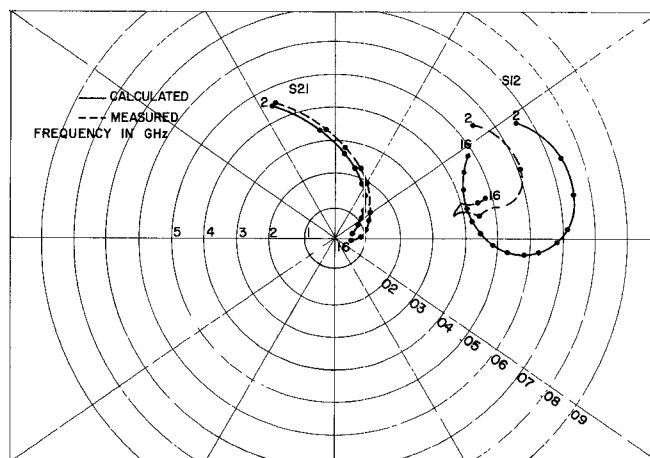Fig. 4. S_{12} and S_{21} for HMF1200.

Fig. 2. Calculated (———) and measured (- - - - -) dc curves for HMF1200.

negative resistance. It has long been known that this phenomenon is due to thermal effects, since the thermal time constant of the MESFET is much smaller than the measurement time (even pulsed measurement). For the HMF1200 the negative slope exists for $V_{gs} > -1$ V. To avoid confusion the negative slope is not included in Fig.

2, and the curves are stopped at the point where the negative slope starts. It can be seen from Fig. 2 that good correlation exists between calculated and measured dc curves. Thermal effects can be included in small-signal analysis by assuming some monotonic decrease of I_{con} with dc power dissipation, and thus correcting the dc point. For large-signal analysis, a similar approach can be adopted. However, here the average power dissipation must be considered. In this paper such a correction was not performed.

The small-signal scattering parameters of the device are presented in Figs. 3 and 4. In Fig. 3, S_{11} and S_{22} are presented and in Fig. 4 S_{12} and S_{21} are presented (calculated—solid line; measured—dashed line). Note the different scales for S_{12} and S_{21} in Fig. 4. The S parameters are for the bias point $V_{DS} = 8$ V, $V_{SG} = 1.5$ V ($\simeq$ 50 percent I_{DSS}). The measured data are taken from the manufacturer's data sheet. Since the HMF1200 is a power MESFET, the large-signal simulation chosen is that of a power amplifier. The amplifier is composed of the device
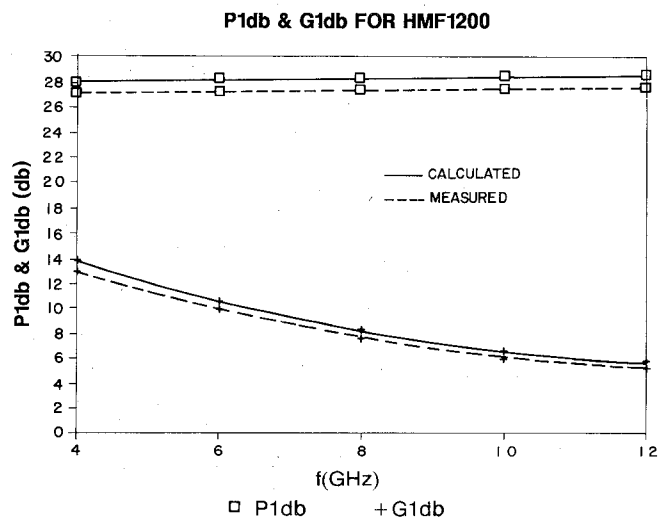
P1db & G1db FOR HMF1200

Fig. 5. 1 dB compression and associated gain for HMF1200 amplifier.

loaded by an optimum power load at the drain and is excited by a power source conjugately matched at the gate. The optimum power load is calculated as outlined in [13]. The input impedance with that load is calculated and the power source is conjugately matched.

The above large-signal network is analyzed using the harmonic balance approach, which is the most useful and efficient method for steady-state applications [1]–[3], [10], [12]. The analysis was performed for the bias point $V_{DS} = 8$ V, $V_{SG} = 1.3$ V (≈ 60 percent I_{DSS}), which is recommended for maximum output power. The analysis was repeated for several power levels up to and beyond the 1 dB compression point and for the frequencies 4, 6, 8, 10, and 12 GHz. The computer program can handle up to eight harmonics in the harmonic balance scheme. However, it was found that three harmonics are sufficient for simulating the network, even beyond the 1 dB compression. Of course, for deep saturation more harmonics are needed. The program runs on an IBM-PC/AT and is very efficient. A typical run takes about 4 seconds for low power levels and increases to 20–25 seconds in the vicinity of the 1 dB compression point.

The results of the simulations are presented in the form of the two graphs in Fig. 5. One graph presents the 1 dB compression point and the other the associated gain versus frequency. The calculated data are presented in the solid line and measured data (from the manufacturer's data sheet) are presented in the dashed line. It can be seen that the calculated gain and power are slightly greater than the measured values. This is expected, since the matching networks have some loss, which is not included in the calculation. The loss in the input matching network may be appreciable due to the large transformation ratio (the input impedance to the device is only a few ohms).

IV. Conclusion

In this paper an improved analytical ac large-signal model for a MESFET is presented. The new model is an upgrading of a previously presented model. The improve-ment is basically in the expressions for the conduction current. Simulation results are presented and compared to measured data.

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